AMENDMENTS TO CLAIMS

The following is a listing of the claims of record with claim 7 amended as shown.

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

Claim 1. (Previously Presented) A flip-chip semiconductor package, comprising:

a first chip carrier mounted with at least a first chip having a first active surface and a first non-active surface opposite to the first active surface wherein a plurality of first solder bumps are formed on the first active surface in direct contact with the first chip carrier for electrically connecting the first chip to the first chip carrier;

a second chip carrier mounted with at least a second chip having a second active surface and a second non-active surface opposite to the second active surface wherein a plurality of second solder bumps are formed on the second active surface in direct contact with the second chip carrier for electrically connecting the second chip to the second chip carrier;

an adhesive layer, applied over the first non-active surface of the first chip for attaching the first non-active surface of the first chip to the second non-active surface of the second chip;

a resin encapsulating layer filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the first and second solder bumps; and

a plurality of conductive vias penetrating the first chip carrier, the resin encapsulating layer, and the second chip carrier so that the second chip carrier forms a direct electrical connection to the first chip carrier via the conductive vias.

2. (Original) The flip-chip semiconductor package of claim 1, wherein a plurality of solder bumps are disposed on the exposed surface of the second chip carrier for forming electrical connection with another semiconductor package.

3.(Original) The flip-chip semiconductor package of claim 1, wherein each of the first chip carrier and the second chip carrier is a substrate.

4.(Original) The flip-chip semiconductor package of claim 1, wherein each of the first chip carrier and the second chip carrier is a tape carrier (TAB).

5. (Original) The flip-chip semiconductor package of claim 1, wherein the adhesive layer is an insulating adhesive having high elasticity.

6. (Original) The flip-chip semiconductor package of claim 1, wherein the resin encapsulating layer is made of resin materials having low hygrosocopicity and low viscosity.

Claim **7. (Currently Amended)** A flip-chip semiconductor package, comprising:

a first chip carrier mounted with at least a first chip having a first active surface and a first non-active surface opposite to the first active surface, wherein a plurality of first solder bumps are formed on the first active surface in direct contact with the first chip carrier for electrically connecting the first chip to first chip carrier;

a second chip carrier mounted with at least a second chip having a second active surface and a second non-active surface opposite to the second active surface,

wherein a plurality of second solder bumps are formed on the second active surface in direct contact with the second chip carrier for electrically connecting the second chip to second chip carrier;

an adhesive layer, applied over the first non-active surface of the first chip for attaching the first non-active surface of the first chip to the second non-active surface of the second chip;

a resin encapsulating layer filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the first and second solder bumps; and

a plurality of conductive traces formed over the first chip carrier, the resin encapsulating layer, and the second chip carrier such that the second chip carrier is electrically connected to the first chip carrier via the conductive traces.

8. (Original) The flip-chip semiconductor package of claim 7, wherein each of the first chip carrier and the second chip carrier is a substrate.

9. (Original) The flip-chip semiconductor package of claim 7, wherein each of the first chip carrier and the second chip carrier is a tape carrier (TAB).

10. (Original) The flip-chip semiconductor package of claim 7, wherein the adhesive layer is an insulating adhesive having high elasticity.

11. (Original) The flip-chip semiconductor package of claim 7, wherein the resin encapsulating layer is made of resin materials having low hygrosocopicity and low viscosity.

12. (Original) The flip-chip semiconductor package of claim 7, wherein each of the conductive traces has one end connected to a second bond pad of the second chip carrier and the other end connected to a first bond pad of the first chip carrier.

13. (Previously Presented) The flip-chip semiconductor package of claim 1, wherein the conductive vias include a plurality of through holes opening through the first chip carrier, the resin encapsulating layer, and the second chip carrier.

14. (Previously Presented) The flip-chip semiconductor package of claim 13, wherein a conductive layer is formed on an inner wall of each of the through holes to define a cavity.

15. (Previously Presented) The flip-chip semiconductor package of claim 14, wherein the conductive layer is made of a copper foil.

16. (Previously Presented) The flip-chip semiconductor package of claim 14, wherein the cavity is filled by a conductive material.

17. (Previously Presented) The flip-chip semiconductor package of claim 14, wherein the cavity is filled by a dielectric material.

18. (Previously Presented) The flip-chip semiconductor package of claim 7, further comprising a dielectric solder mask for encapsulating the conductive traces.